REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

The specification is amended by the present response to correct minor grammatical and idiomatic informalities. The changes made to the specification are deemed to be self-evident from the original disclosure, and thus are not deemed to raise any issues of new matter.

Claims 1-16 are pending in this application. Claim 1 was rejected under 35 U.S.C. § 102(e) as anticipated by U.S. patent 5,519,652 to Kumakura et al. (herein "Kumakura"). Claims 2-16 were objected to as dependent upon a rejected base claims but were noted as allowable if rewritten in independent form to include all of the limitations of their base claim and any intervening claims.

Initially, applicants gratefully acknowledge the indication of the allowable subject matter in claims 2-16.

Addressing now the rejection of claim 1 under 35 U.S.C. § 102(e) as anticipated by Kumakura, that rejection is traversed by the present response.

Independent claim 1 is amended by the present response to clarify that the MOS transistor in the memory cell includes "diffusion layers formed at said device substrate and a body between the diffusion layers, said body being in an electrically floating state to store data...". That subject matter is believed to be clear from the original specification, for example see the disclosure in the present specification at page 5, line 19 to page 6, line 15. The claimed structure is believed to also clearly distinguish over the disclosure in Kumakura.

Kumakura is directed to a non-volatile semiconductor memory in which each of memory cells is a MIS transistor formed at an intersection at word and bit lines.

Applicants first note that in independent claim 1 the device substrate has "a semiconductor layer separated by a dielectric layer from a base substrate". Applicants

respectfully submit Kumakura does not disclose that feature. With respect to that feature the outstanding Office Action cites the Abstract of Kumakura, but in the Abstract Kumakura merely discloses the use of MIS transistor cells, and fails to disclose on what kind of substrate the memory cells are formed. Thus, Kumakura does not in fact disclose "a device substrate having a semiconductor layer separated by a dielectric layer from a base substrate".

Further, Kumakura does not disclose the now clarified structure of each memory cell having a MOS transistor including "diffusion layers formed at said device substrate and a body between the diffusion layers, said body being in an electrically floating state to store data...".

With respect to that feature the outstanding rejection cites Figure 1 in Kumakura. However, in Figure 1 Kumakura discloses a so-called stacked gate transistor memory cell. Such a structure does not, however, meet the claimed limitations. More particularly, a floating gate in the stacked gate transistor memory cell is formed on a semiconductor substrate via an insulator film.

In contrast to such a structure as in Kumakura, the claimed "body" in the electrically floating state is formed between diffusion layers formed at a device substrate. Thus, the structure of the claimed "body" differs from the noted "floating gate" in Figure 1 of Kumakura.

In such ways, Kumakura also does not disclose the further claimed feature of the MOS transistor including "diffusion layers formed at said device substrate at a body between the diffusion layers, said body being in an electrically floating state to store data...".

In view of these foregoing comments, applicants respectfully submit independent claim 1 recites features neither taught nor suggested by Kumakura, and thus independent claim 1 also distinguishes over Kumakura.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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